

What is claimed is:

1 1. A method of filling a bit line contact via,
2 comprising:

3 providing a substrate having a device region and
4 periphery region, the device region having a
5 transistor with a gate electrode, drain region,
6 and source region on the substrate;

7 forming a dielectric layer overlying the substrate, the
8 dielectric layer having a bit line contact via
9 exposing the drain region, and periphery contact
10 via exposing the periphery region;

11 forming a doped conductive layer, lower than the
12 dielectric layer, overlying the drain region;

13 conformally forming a barrier layer overlying the
14 dielectric layer, doped conductive layer, and
15 periphery region; and

16 forming a first conductive layer filling the bit line
17 contact via and periphery contact via.

1 2. The method as claimed in claim 1, wherein the
2 dielectric layer is oxide.

1 3. The method as claimed in claim 1, wherein the doped
2 conductive layer is polycrystalline silicon doped with As.

1 4. The method as claimed in claim 1, wherein forming
2 the doped conductive layer further comprises:

3 forming the doped conductive layer overlying the drain
4 region, dielectric layer, and periphery region;
5 and

6 removing the doped conductive layer by etching, thereby
7 leaving a doped conductive layer overlying the
8 drain region.

1 5. The method as claimed in claim 1, wherein the
2 barrier layer prevents the diffusion of the first
3 conductive layer.

1 6. The method as claimed in claim 1, wherein the
2 barrier layer comprises a TiN layer.

1 7. The method as claimed in claim 1, wherein the first
2 conductive layer is tungsten.

1 8. The method as claimed in claim 1, wherein the
2 periphery region is a doped region.

1 9. The method as claimed in claim 1, wherein the
2 periphery region is a second conductive layer, and the gate
3 electrode further comprises the second conductive layer.

1 10. The method as claimed in claim 9, wherein the
2 second conductive layer is a silicide layer comprising
3 tungsten.

1 11. A method of a filling bit line contact via,
2 comprising:

3 providing a substrate having a device region and
4 periphery region, the device region having a
5 transistor with a gate electrode, drain region,
6 and source region on the substrate;
7 forming a dielectric layer overlying the substrate, the
8 dielectric layer having a bit line contact via

9 exposing the drain region, and periphery contact
10 via exposing the periphery region;
11 forming a doped conductive layer overlying the drain
12 region, dielectric layer, and periphery region;
13 removing the doped conductive layer using etching,
14 thereby remaining the doped conductive layer,
15 lower than the dielectric layer, overlying the
16 drain region;
17 conformally forming a barrier layer overlying the
18 dielectric layer, doped conductive layer, and
19 periphery region; and
20 forming a first conductive layer filling the bit line
21 contact via and periphery contact via.

1 12. The method as claimed in claim 11, wherein the
2 dielectric layer is an oxide layer.

1 13. The method as claimed in claim 11, wherein the
2 doped conductive layer is polycrystalline silicon doped with
3 As.

1 14. The method as claimed in claim 11, wherein the
2 barrier layer prevents the diffusion of the first conductive
3 layer.

1 15. The method as claimed in claim 11, wherein the
2 barrier layer comprises a TiN layer.

1 16. The method as claimed in claim 11, wherein the
2 first conductive layer is tungsten.

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1 17. The method as claimed in claim 11, wherein the
2 periphery region is a doped region.

1 18. The method as claimed in claim 11, wherein the
2 periphery region is a second conductive layer, and the gate
3 electrode further comprises the second conductive layer.

1 19. The method as claimed in claim 18, wherein the
2 second conductive layer is a silicide layer comprising
3 tungsten.